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10/31/2005

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LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035

Date October 31, 2005

Number of pages including cover sheet 3

To: US PTO, Mail Stop Issue Fee

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From: Connie del Castillo

Intellectual Property Paralegal

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No. _____

Fax No. (408) 433-7460

REMARKS:

☐ Urgent ☐ For your review ☐ Reply ASAP ☐ Please comment

Application Number: 10/676,602
Filing date: October 1, 2003
First named inventor: Jau-Wen Chen et al.
Attorney docket number: 03-0717

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Connie del Castillo	(Depositor's name)
<i>Connie del Castillo</i>	(Signature)
10/31/05	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,602	10/01/2003	Jau-Wen Chen	03-0717	7921

TITLE OF INVENTION: SUBSTRATE-BIASED I/O AND POWER ESD PROTECTION CIRCUITS IN DEEP-SUBMICRON TWIN-Well PROCESS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	11/10/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
WARREN, MATTHEW E	2815	257-356000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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Trexler, Bushnell,
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3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT. (print or type)

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(A) NAME OF ASSIGNEE

LSI Logic Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Milpitas, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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Authorized Signature

Timothy Croll

Date

28 Oct 05

Typed or printed name

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36,771

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